UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,543	09/24/2004	Hsin-Chung Huang	13528-US-PA	5542

31561 7590 07/12/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
KOVALICK, VINCENT E	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
07/12/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/711,543	HUANG ET AL.	
	Examiner	Art Unit	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3 and 7-14* is/are allowed.

6)☒ Claim(s) *4 and 6* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Patent Application, Serial No. 10/711,543, with a File Date of September 24, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deane et al., Pub. No. 2006/0097965. taken with Sakashita et al. Pub No. 2004/0169665 in view of Iwasaki, Pub. No. 2004/0179315).

Relative to claim 4, Deane et al. **teaches** an active matrix electroluminescent display device (pg. 1, paras. 0001-0008); Deane et al. further **teaches** a method of discharging pixel transistors of an LCD device (pg. 3, para. 0028).

Deane et al. **does not teach** detecting whether the LCD device stops displaying an image; providing a first signal to disable a power module of the LCD device and turn off a pixel transistor turn-on potential level after a first delay time; and providing a second signal to turn on all the pixel transistors after a second delay time.

Sakashita et al. **teaches** an image display device and method of displaying an image on the basis of a plurality of image signals (pg. 2, paras. 0018-0021); Sakashita e al further **teaches** detecting whether the LCD device stops displaying an image; providing a first signal to disable a power module of the LCD device and turn off a pixel transistor turn-on potential level after a first delay time (pg. 4, para. 0076).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Deane et al. the feature as taught by Sakashita e al. in order to provide the logic means to determine weather of not the LCD device stop displaying and image.

Deane et al. taken with Skashita et al. **does not teach** providing a second signal to turn on all the pixel transistors after a second delay time.

Iwasaki **teaches** and LCD power source control method and control circuit thereof (pgs. 2/3/4, paras. 0024-0044); Iwasaki further **teaches** providing a second signal to turn on all the pixel transistors after a second delay time (pg. 8, paras. 0108 and pg. 11, para. 0153).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the methodology as taught by Deane et al. taken with Sakashita the feature as taught by Iwasaki in order to turn on the power to activate the display pixels in the proper time sequence.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deane et al., taken with Sakashita et al. in view of Iwasaki as applied to claim 4 in item 3 hereinabove, and further in view of Nakajima et al. (Pub. No. 2004/0183772).

Regarding claim 6, Deane et al., taken with Sakashita et al. in view of Iwasaki **does not teach** the method practice wherein the pixel transistors are fabricated by utilizing Thin Film Transistor (TFT) technology.

Nakajima et al. **teaches** flat-panel display devices as typified by liquid crystal display devices and EL (electroluminescence) display devices (pg. 1, paras. 0002-0008); Nakajima et al. further **teaches** the method practice wherein the pixel transistors are fabricated by utilizing Thin Film Transistor (TFT) technology (pg. 1, para. 0002).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Deane et al. taken with Sakashita et al. in view of Iwasaki, the feature as taught by Nakajima et al. in order to produce LCD panels having improved resolution and increased speed.

Allowable Subject Matter

5. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Relative to claim 5, the major difference between the teachings of the prior art of record (Deane et al., Pub. No. 2006/0097965; Sakashita et al., Pub No. 2004/0169665 and Iwasaki, Pub. No. 2004/017931) and that of the instant invention is that said prior art of record **does not teach** a method of discharging pixel transistor of an LCD device by assigning a start point of an all-gate-on period of all the pixel transistor after an analog voltage source supplying the LCD device is reduced to a ground voltage level, such that the pixel transistors are discharged via sources thereof within the first delay time; and assigning an end point of the all-gate-on period of all the pixel transistor before the pixel transistor turn-on level reaches to a threshold voltage for turning on the pixel transistors.

6. Claims 1-3 and 7-14 are allowed.

7. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a control circuit, for an LCD device having a power module, a host control unit, and an image display unit, the power module supplying a plurality of potential levels for the LCD device, the control unit controlling a plurality of gate driving signals and a plurality of source driving signals for the image display unit, the control circuit comprising: a signal delay unit, coupled to the image display unit; and a signal detecting unit, coupled to the host control unit, wherein the signal detecting unit detects an on/off status of the LCD device from the host control unit, provides a disable signal to the power module, such that the voltage potential levels are disabled except a pixel transistor turning-on level, a plurality of pixel transistors of the image display unit are discharged via sources of the pixel transistors, and provides an all-gate-on signal to the signal delay unit, the all-gate-on signal is delayed for a first delay time by the signal delay unit and outputs to the image display unit.

Relative to claim 7, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an Applied Specific Integrated Circuit (ASIC), for a capacitor charging/discharging device, having a plurality of capacitors, comprising: a host control unit; a signal detecting unit, receiving a first disable signal outputted from the host control unit and outputting a second disable signal to a power supply module outside of the ASIC, for disabling a part of the power supply module simultaneously, and disabling other part of the power supply module which controls the capacitors after a first delay time; and a delay unit, receiving a second signal from the signal detecting unit, and outputting to the capacitor charging/discharging device after having paused for a second delay time, such that a plurality of switches controlling the capacitors are turned on.

Regarding claim 8, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** an LCD panel system, for operating an LCD panel controlled by at least a plurality of source driving signals and a plurality of gate driving signals, comprising: a control circuit, outputting a plurality of data and a plurality of control signals; a pixel array, coupled to the control circuit, having a plurality of pixels arranged in an array, wherein each of the pixels corresponds to a transistor for receiving at least one of the data provided from the control circuit and at least one of the control signals for displaying an image; a power module, for supplying a plurality of potential levels to the LCD panel and receiving at least a part of the control signals from the control circuit, wherein when the control circuit detects the LCD panel has stopped to display the image, a first signal and a second signal are transmitted, wherein the first signal disables the power module and turns off a pixel transistor turn-on level after a first delay time, and the second signal turns on gates of the transistors corresponding to all of the pixels after a second delay time.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No.	US 2004/0147113	Yamazaki et al.
Pub. No.	US 2003/0234780	Hsieh et al.
Pub. No.	US 2003/0146907	Boals et al.
Pub. No.	US 2002/0158587	Komiya

To Respond

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Vincent E. Kovalick
June 27, 2007